## IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method of transferring a data stream comprising:

directly transferring a plurality of bits associated with a data stream from [[a]] an external data source to a temporary storage;

concurrently intercepting during the transfer each bit associated with the data stream and counting a bit-transfer total and a bit-set total associated with the data stream; and

determining if the bit-set total exceeds more than half the bit-transfer total and if so setting an inversion flag bit which is associated with the data stream, and wherein the processing of the method and the temporary storage reside within a same controller as one another.

2. (Original) The method of claim 1, further comprising:

transferring from the temporary storage to a target source each bit associated with the data stream and concurrently inverting each bit as transferred, if the inversion flag bit is set.

3. (Original) The method of claim 1, further comprising:

shifting the inversion flag bit to a flag storage.

4. (Original) The method of claim 3, further comprising:

assembling one or more additional inversion flag bits in the flag storage, each additional inversion flag bit associated with a single additional data stream; and

maintaining each additional data stream in the temporary storage.

5. (Original) The method of claim 4, further comprising:

transferring from the temporary storage to a target source each bit associated with the data stream and each of the additional data streams while concurrently inverting each transferred

bit, if the inversion flag bit associated with a transferred data stream is set, as identified in the flag storage.

6. (Original) The method of claim 5, wherein the flag storage is a register.

7. (Currently Amended) A method of transferring a data stream, comprising:

directly receiving a data stream and an inversion flag associated with the data stream from [[a]] an external data source;

transferring one or more bits associated with the data stream from a data source to a target source, if the inversion flag is unset; and

inverting the bits associated with the data stream as the data stream is transferred from the data source to the target source, if the inversion flag is set, wherein the data stream is processed and temporarily housed in storage within a same controller as it is transferred to the target source.

8. (Original) The method of claim 7, wherein the inversion flag and the data stream are stored together in the data source.

9. (Original) The method of claim 7, wherein the inversion flag and the data stream are separately stored in the data source.

10. (Original) The method of claim 7, wherein the inversion flag is stored with one or more additional inversion flags as a single data structure in the data source, each additional inversion flag associated with an additional data stream.

11. (Currently Amended) A computer readable medium having executable instructions for executing a method which is operable to invert transferred data, the method comprising:

acquiring a data stream and an inversion flag directly from [[a]] an external data source;

separating the data stream and the inversion flag into a data stream storage and an inversion flag storage; and

buffering one or more additional data streams and one or more additional inversion flags from the data source in the storages, within a same controller.

12. (Original) The medium of claim 11, further comprising:

inverting all bits associated with a transferred data stream as the transferred data stream is sent to a target source from the data stream storage, if a corresponding inversion flag associated with the transferred data stream is set in the inversion flag storage.

13. (Currently Amended) A data structure implemented in a computer readable medium operable to be transferred from a data source, comprising:

a data stream having a plurality of bits; and

an inversion bit associated with the data stream which is set after the data stream is transferred to a temporary storage, the inversion bit is set by [[a]] an external data source if a total number of set data stream bits exceeds more than half a total number of bits associated with the data stream, wherein the total numbers are tabulated concurrently as the data stream is transferred to the temporary storage, and wherein if the inversion bit is set then a state within the data source is changed permitting the data stream to be inverted when directly transferred from the data source to a target source, and wherein the temporary storage resides within a same controller as the processing to invert the data stream.

14. (Previously Presented) The data structure of claim 13, further comprising:

an inversion bit stream including the inversion bit and one or more additional inversion bits, each additional inversion bit associated with an additional data stream.

15. (Previously Presented) The data structure of claim 14, wherein the data stream and the additional data streams are transferred from the temporary storage to the target source, and wherein during the transfer the transferred bits associated with the transferred data stream are inverted if a corresponding inversion bit or additional inversion bit associated with the transferred data stream is set.

16. (Previously Presented) The data structure of claim 13, wherein the bits of the data stream are inverted if the inversion bit is set during a transfer of the data stream from the temporary storage to the target source.

17. (Currently Amended) An inversion data transfer system, comprising:

[[a]] an external data source device;

a temporary storage; and

a controller that directly transfers a data stream having a plurality of bits from the data source device to the temporary storage, and concurrent to the transfer determines if a total number of set bits within the data stream is more than half of a total number of bits associated with the data stream, and if so associating a set inversion bit with the data stream, otherwise associating an unset inversion bit with the data stream, wherein the temporary storage resides within the controller.

18. (Original) The system of claim 17, further comprising:

a target source device which concurrently receives the bits of the data stream inverted, as the data stream is transferred from the temporary storage, if a set inversion bit associated with the data stream is detected.

19. (Original) The system of claim 17, further comprising:

a register storage operable to house the inversion bit and one or more additional inversion bits, wherein each additional inversion bit is associated with an additional data stream.

20. (Original) The system of claim 19, wherein the controller further retrieves from the register storage each inversion bit associated with a transferred data stream and is operable to concurrently transfer the transferred data stream from the temporary storage and invert the bits associated with the transferred data stream if the inversion bit is set.

21. (Currently Amended) An inversion data transfer system, comprising:

[[a]] an external data source device;

a target source device; and

a controller that directly acquires a data stream and an inversion bit associated with the data stream from the data source device and inverts bits associated with the data stream during a transfer of the data stream to a target source device, if the inversion bit is set, and wherein the controller buffers the data stream before it is transferred to the target source device within the controller.

22. (Original) The system of claim 21 further comprising:

a temporary storage operable to house the data stream as the data stream is acquired from the data source device; and

a register storage operable to house the inversion bit as the data stream is acquired from the data source device.

23. (Previously Presented) The system of claim 21, wherein the controller acquires the inversion bit by stripping the inversion bit from the data stream.

24. (Original) The system of claim 21, wherein the controller acquires the inversion bit as a separate data structure having one or more additional inversion bits with each additional inversion bit being associated with a single additional data stream.

25. (Currently Amended) A system for transferring a data stream, comprising:

a control buffer;

a storage buffer;

an inversion storage;

a counting set of executable instructions to count set bits associated with a data stream being received from the control buffer into the storage buffer as the storage buffer directly receives the data stream from [[a]] <u>an external</u> data source, and the counting set of executable instructions generates an inversion bit associated with the data stream, wherein the inversion bit is housed in the inversion storage and is set if a total number of set bits exceeds more than half a

total number of bits associated with the data stream, and wherein the inversion storage, the storage buffer, and the counting set of instructions reside within a same controller.

26. (Original) The system of claim 25, further comprising:

a transfer set of executable instructions operable to use the counting set of executable instructions to transfer the data stream from the storage buffer to a target device, wherein the entire data stream is inverted if the inversion bit is set as the data stream is being transferred to the target device.

27. (Original) The system of claim 26, wherein the inversion bit is transferred with the data stream to the target device.

28. (Currently Amended) A memory apparatus, comprising:

a controller that directly acquires a data packet and an associated inversion bit from [[a]] an external data source and transfers the packet and concurrently inverts the packet if the inversion bit is set.

29. (Original) The apparatus of claim 28, wherein the controller buffers the packet prior to transfer.

30. (Original) The apparatus of claim 29, wherein the controller separates the packet and the inversion bit.

31. (Original) The apparatus of claim 30, wherein the inversion bit is housed in a register prior to the transfer.

32. (Original) The apparatus of claim 28, wherein the controller acquires the inversion bit by counting set bits associated with the data packet, as the packet is acquired.

33. (Currently Amended) A memory apparatus, comprising:

an inversion bit;

a data packet;

a state machine that controls the transfer of the data packet to a target device wherein the packet is inverted as it is transferred to the target device, if the inversion bit is set, and wherein the state machine directly receives the data packet from [[a]] an external data source and processes the data packet within the apparatus.

34. (Original) The apparatus of claim 33, further comprising:

a buffer to house the data packet prior to transfer to the target device; and

a register to house the inversion bit.

35. (Original) The apparatus of claim 33, wherein the state machine is configured by interfacing one or more electro-mechanical devices.

36. (Original) The apparatus of claim 33, wherein the state machine is configured using a set of executable instructions.

37. (Original) The apparatus of claim 33, wherein the data packet is a fixed length data packet.

38. (Original) The apparatus of claim 33, wherein the data packet is a variable length data packet.

39. (Original) The apparatus of claim 33, wherein the apparatus is a flash memory device.

40. (Currently Amended) A flash memory device, comprising:

a temporary storage;

a receiving controller;

a counting controller; and

a transferring controller that transfers a data packet directly received by the receiving controller in a temporary storage to [[a]] an external target device and further inverts the data packet during the transfer if the counting controller indicates to the transferring controller that the packet requires inversion, and wherein the counting controller and the temporary storage reside within the transferring controller.

41. (Original) The flash memory device of claim 40, wherein the counting controller indicates the packet requires inversion if a total number of set bits associated with the packet exceeds more than half a total number of bits associated with the packet.

42. (Original) The flash memory device of claim 40, wherein the memory device is at least one of a compact flash memory card and a multimedia card.

43. (Original) The flash memory device of claim 40, wherein the memory device is included in the operation of a at least one of a digital camera device, digital video device, and a portable audio player device.

44. (Original) The flash memory device of claim 40, wherein the counting controller includes a packet based ones counter.

45. (Original) The flash memory device of claim 40, further comprising a shift-load register used to house an inversion bit generated by the counting controller, wherein the inversion bit, if set, indicates the data packet is to be inverted.

46. (Original) The flash memory device of claim 45, wherein one or more multiplexers, the shift-load register, and the temporary storage are used by the transferring controller to transfer the data packet.